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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/816,204	04/01/2004	Francesco La Rosa	852663.411	7568

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EXAMINER	
AUDUONG, GENE NGHIA	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 07/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/816,204	LA ROSA, FRANCESCO	
	Examiner	Art Unit	
	Gene N. Auduong	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-18 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-18 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 8-16-2004.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on August 16, 2004 is being considered by the examiner.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

4. Claims 1-18 are rejected under 35 U.S.C. 102(a) as being anticipated by Perner et al. (U.S. Pat. No. 6,501,697).

Regarding claims 1 and 18, Perner et al. disclose a sense amplifier for reading a memory cell (figure 4), comprising: a read node electrically coupled to the memory cell (read node on the sense side, left side, of the sense amplifier 38); a first active branch (memory branch) connected to the read node and comprising means for supplying a read current at the read node; and a data output linked to one node of the first active branch at which a voltage representative of the conductivity state of the memory cell appears (data of the memory branch output via the amplifier 76), a second active branch connected to the read node, comprising means for supplying, at the read node, a current that is added to the current supplied by the first active

branch, such that the voltage representative of the conductivity state of the memory cell remains substantially stable upon a current draw at the read node (col. 6, lines 1+).

Regarding claim 2, Perner et al. disclose the sense amplifier according to claim 1 wherein the first active branch is off and does not supply any current during the reading of an off or barely conductive memory cell (col. 6, lines 26+).

Regarding claim 3, Perner disclose the sense amplifier according to claim 1 wherein the first active branch comprises a first current generator linked to the read node, and the second read branch comprises a second current generator linked to the read node (col. 6, lines 26+).

Regarding claim 4, Perner et al. disclose the sense amplifier according to claim 3 wherein the current generators comprise PMOS transistors driven by a common reference voltage (col. 7, lines 1+).

Regarding claim 5, Perner et al. disclose the sense amplifier according to claim 3 Wherein the second current generator supplies a current higher than a current supplied by the first current generator (col. 6, lines 29+).

Regarding claim 6, Perner et al. disclose the sense amplifier according to claim 3 wherein the first current generator is linked to the read node through at least a first cascode transistor, and the second current generator is linked to the read node through at least a second cascode transistor (col. 6, lines 1+).

Regarding claim 7, Perner et al. disclose the sense amplifier according to claim 3 wherein the first current generator is linked to the read node through at least a first MOS transistor, while the second current generator is linked directly to the read node, the read node being connected to a voltage-limiting diode (col. 6, lines 29+).

Regarding claim 8, Perner et al. disclose the sense amplifier according to claim 1, further comprising: a stage for controlling the first and the second active branches (figure 3, controller 44).

Regarding claim 9, Perner et al. disclose the sense amplifier according to claim 8 wherein the control stage controls the active branches such that a voltage appearing at the read node is regulated in the vicinity of a predetermined value.(col. 5, lines 29+).

Regarding claim 10, Perner et al. disclose the sense amplifier according to claim 8 wherein the control stage controls the active branches such that the first active branch does not supply current while the current supplied by the second active branch does not supply the maximum value of the current it can deliver (col. 5, lines 29+).

Regarding claim 11, Perner et al. disclose the sense amplifier according to claim 8 wherein: the control stage supplies a first gate control voltage to a first cascode transistor of the first active branch, and a second gate control voltage to a second cascode transistor of the second active branch, and the first and second control voltages are controlled by the control stage such that the gate source voltage of the second transistor is higher than the gate source voltage of the first transistor (col. 5, lines 29+).

Regarding claim 12, Perner et al. disclose the sense amplifier according to claim 11 wherein: the first and second cascode transistors are N-type MOS transistors; and the second control voltage is higher than the first control voltage (col. 6, lines 42+).

Regarding claim 13, Perner et al. disclose the sense amplifier according to claim 11 wherein: the control stage comprises a current generator in series with a load; the first control

voltage is taken off at the cathode of the load; and the second control voltage is taken off at the anode of the load (figure 4).

Regarding claim 14, Perner et al. disclose the sense amplifier according to claim 13 wherein the load is a resistance (figure 4).

Regarding claim 15, Perner et al. disclose the sense amplifier according to claim 13 wherein the load is a MOS transistor (figure 4, col. 6, lines 1+).

Regarding claim 16, Perner et al. disclose the sense amplifier according to claim 1, further comprising a precharge transistor for supplying, during a precharge phase, a precharge current higher than the sum of the currents supplied by the first and the second active branches (col. 6, lines 60+).

Regarding claim 17, Perner et al. disclose the non-volatile memory comprising a memory array 30 comprising at least one memory cell 36, characterized in that it further comprises at least one sense amplifier 38 according to claim 1 for reading the memory cell (figure 3).

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gene N. Auduong whose telephone number is (571) 272-1773. The examiner can normally be reached on 9-5-4, alternate second Monday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho can be reached on (571) 272-1777. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GA
July 11, 2005

Gene N Auduong
Primary Examiner
Art Unit 2827